METHOD OF FABRICATING THIN FILM TRANSISTOR ARRAY

DESCRIPTION

CROSS-REFERENCE TO RELATED APPLICATION

[Para 1] This application is a divisional of a prior application serial no. 10/249,340, filed April 02, 2003, which claims the priority benefit of Taiwan application serial no. 91135000, filed December 03 2002.

BACKGROUND OF THE INVENTION

[Para 2] Field of Invention

[Para 3] The present invention relates to a method of fabricating the thin film transistor array inside a liquid crystal display (LCD). More particularly, the present invention relates to a method of fabricating a thin film transistor array that minimizes damages due to electrostatic discharge (ESD).

[Para 4] Description of Related Art

[Para 5] Liquid crystal display (LCD) has many advantages over a cathode ray tube (CRT) such as a low operating voltage, radiation free, light and occupying a small volume. LCD together with other flat panel type display such as plasma displays and electroluminance displays has become one of the most researched types of displays. At present, active matrix liquid crystal display is often regarded as having the greatest potential to become a next generation product. However, as the number of scan lines is increased, duty cycles assigned by an external driver to each pixel will be reduced. Hence, there will be continuous deterioration of display properties in the display device.

[Para 6] An active array liquid crystal display has a transistor or a diode in each pixel electrode to serve as an active element controlling the writing of data into the liquid crystal display. Currently, thin film transistor liquid crystal display is regarded as the mainstream among other liquid crystal displays. When a pixel electrode is selected (that is, in an 'on' state), signal is written into the pixel. On the other hand, when the pixel electrode is de-selected (that is, in an 'off' state), a storage capacitor within each pixel unit maintains a potential in the liquid crystal layer within the display. Consequently, the liquid crystal and the duty cycle have a static property.

[Para 7] In general, the thin film transistor array within a thin film transistor display is fabricated using a 'five photomask' process as shown in Figs. 1A to 1E. The photomask process includes operations such as photoresist coating, soft baking, hard baking, photo-exposure, photoresist fixing, chemical development and etching so that various thin films are patterned.

[Para 8] Figs. 1A to 1E are schematic cross-sectional view showing the steps for fabricating conventional thin film transistor array. As shown in Fig. 1A, a first photomask is used to form a first metallic layer 102 over a substrate 100. The first metallic layer 102 is a patterned metallic layer comprising a gate 102a and a gate connected scan line 102b.

[Para 9] As shown in Fig. 1B, a gate insulating layer 104 is formed over the gates 102a and the scan lines 102b over the substrate 100. Thereafter, a second photomask is used to form a channel layer 106 over the gate insulating layer 104 that crosses over the gate 102a.

[Para 10] As shown in Fig. 1C, a third photomask is used to form a second metallic layer 110 over the substrate 100. The second metallic layer 110 mainly includes a source/drain 110a and a data line 110b with connection to one of the source/drain 110 terminals (the source terminal). In addition, the source/drain 110a are located on each side of the channel layer 106.

[Para 11] As shown in Fig. 1D, a passivation layer 112 is formed over the substrate 100 covering the thin films, that is, the first metallic layer 102, the gate insulating layer 104, the channel layer 106, the second metallic layer 110.

A fourth photomask is used to form contact openings 114 in the passivation layer that expose the other terminal (the drain terminal) of the source/drain 110a.

[Para 12] As shown in Fig. 1E, a fifth photomask is used to form a pixel electrode 116 over the passivation layer 112. The pixel electrode 116 may be fabricated using a material such as indium-tin oxide or indium-zinc oxide. Furthermore, the pixel electrode 116 is electrically connected to the other terminal (the drain terminal) of the source/drain 110a through the contact opening 114 in the passivation layer 112.

[Para 13] Aside from forming contact openings 114 in the fourth photomask step, openings 115a and 115b are also formed in the gate insulating layer 104 and the passivation layer 112 close to the edge of the substrate 100 as shown in Fig. 1F. Fig. 1F is a cross-section through a peripheral area of Fig. 1E. The openings 115a and 115b expose the first metallic layer 102 and the second metallic layer 110. The first metallic layer 102 and the second metallic layer 110 are electrically connected through the pixel electrode 116 only after the fifth photomask step is completed. In other words, before conductive the fourth photomask step, the first metallic layer 102 and the second metallic layer 110 are isolated from each other. Hence, the probability of having an electrostatic discharge (ESD) between the two metallic layers is rather high.

[Para 14] One method to reduce possible damages due to an ESD between the two metallic layers includes conducting one more photomask step to pattern the gate insulating layer. The patterned gate insulating layer has a short ring opening that exposes the first metallic layer electrically. The short ring opening permits an electrical connection of the subsequently formed second metallic layer with the underlying first metallic layer. However, this will increase the number of photomask step by one and hence add processing complexity as well as production cost.

SUMMARY OF THE INVENTION

[Para 15] Accordingly, one object of the present invention is to provide a method of fabricating a thin film transistor array capable of preventing damage due to an electrostatic discharge between a first metallic layer and a second metallic layer prior to the formation of a pixel electrode in a conventional process.

[Para 16] A second object of this invention is to provide a method of fabricating thin film transistor capable of preventing damage due to an electrostatic discharge between a first metallic layer and a second metallic layer without increasing processing steps or production cost.

[Para 17] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a method of fabricating a thin film transistor array. The method is suitable for fabricating a thin film transistor array on a substrate having at least one designated display region. The method includes forming a first patterned conductive layer over the substrate. The first patterned conductive layer distributes over an area range exceeding the designated display region. Thereafter, a first dielectric layer is formed over the substrate. Through the first dielectric layer, the patterned conductive layer outside the designated display region is exposed. A second patterned conductive layer is formed over the first dielectric layer. The second patterned conductive layer and the exposed first patterned conductive layer are electrically connected. A second dielectric layer is formed over the substrate. The second dielectric layer has a plurality of contact openings. A plurality of pixel electrodes is formed over the second dielectric layer such that the pixel electrode and the second patterned conductive layer are electrically connected through the contact openings. Finally, the second dielectric layer, the second patterned conductive layer, the first dielectric layer and the first patterned conductive layer outside the designated display region are removed.

[Para 18] This invention also provides a method of eliminating damages caused by electrostatic discharge that can be applied to the fabrication of a thin film transistor array on a designated display region. The thin film transistor array includes a first patterned conductive layer having an area

distribution range exceeding the designated display region and including a plurality of gates and a plurality of gate connected scan lines, a second patterned conductive layer over the first patterned conductive layer having a plurality of source/drain terminals and source/drain terminal (source terminal) connected data lines, a pixel electrode between the first patterned conductive layer and the second patterned conductive layer and a pixel electrode connected to the source/drain terminal (the drain terminal). One major aspect of this invention is that in the process of forming the first dielectric layer, the first dielectric layer covers the gates and the scan lines inside the designated display region but exposes the first patterned conductive layer outside the designated display region. Thereafter, in the process of forming the second patterned conductive layer over the first patterned conductive layer, the second patterned conductive layer and the exposes first patterned conductive layer are electrically connected.

[Para 19] The step of forming the first dielectric layer includes using a chemical vapor deposition and controlling the processing parameters such that the first dielectric layer only covers the gates and the scan lines inside the designated display region but exposes the first patterned conductive layer outside the designated display region. The first dielectric layer has a thickness getting smaller toward the edge.

[Para 20] This invention also provides a thin film transistor array semi-finished product structure suitable for forming on a substrate having at least one designated display region. The semi-finished product structure includes a first patterned conductive layer, a dielectric layer and a second patterned conductive layer. The first patterned conductive layer is positioned over the substrate and distributed over an area range exceeding the designed display region. The dielectric layer covers a portion of the first patterned conductive layer but exposes the first patterned conductive layer outside the designated display region. The second patterned conductive layer is positioned over the dielectric layer. The second patterned conductive layer and the exposed first patterned conductive layer are electrically connected.

[Para 21] In this invention, the second patterned conductive layer and the first patterned conductive layer are electrically connected before forming the source/drain terminals and the data lines. Hence, probability of having a damaging electrostatic discharge before the fabrication of the pixel electrode is greatly minimized. Furthermore, this invention need no additional photomask step and hence able to avoid possible damage to the thin film transistor device caused by an electrostatic discharge between the electrically isolated first and second metallic layer in a conventional fabrication process.

[Para 22] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[Para 23] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

[Para 24] Figs. 1A to 1E are schematic cross-sectional view showing the steps for fabricating conventional thin film transistor array;

[Para 25] Fig. 1F is a cross-section through a peripheral area of Fig. 1E;

[Para 26] Figs. 2A to 2C are top views showing the front-end fabrication process of a thin film transistor array according to one preferred embodiment of this invention;

[Para 27] Fig. 3A is a magnified view of section III in Fig. 2B,

[Para 28] Fig. 3B is a simplified sectional view of Fig. 2C;

[Para 29] Fig. 3C is a magnified view of section III' in Fig. 2C; and

[Para 30] Figs. 3D and 3E are top views showing the steps carried out after fabricating the thin film transistor array structure as shown in Fig. 3B.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[Para 31] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[Para 32] Figs. 2A to 2C are top views showing the front-end fabrication process of a thin film transistor array according to one preferred embodiment of this invention. As shown in Fig. 2A a substrate 200 having a plurality of designated display regions 201 is provided. In this embodiment, the designated display regions refer to the areas on the substrate 200 for forming display panels. Here, although six display regions 201 are shown, the number of display regions on a substrate 200 is unrestricted. Thereafter, a first patterned conductive layer 202 is formed over the substrate 200. The first patterned conductive layer 202 distributes over an area range that exceeds the display regions 201. The first patterned conductive layer 202 includes a plurality of gates 202a and a plurality of gate connected scan lines 202b. The process of forming the first patterned conductive layer 202 includes depositing conductive material over the substrate 200 to form a first conductive layer (not shown) and then conducting photolithographic and etching process to pattern the first conductive layer. The first conductive layer is formed, for example, by sputtering a metallic material such as chromium or tantalum. To simplify the figure, only one of the scan lines 202b and one of the gates 202a over the scan lines 202b is shown inside each designated display region 201. In practice, however, each designated display region 201 should include more than one scan line 202b.

[Para 33] As shown in Fig. 2B, a first dielectric layer 204 is formed over the substrate 200 to serve as a gate insulating layer. The first dielectric layer 204 covers the gates 202a and the scan lines 202b inside the designated display regions 201 but exposes the first patterned conductive layer 202 outside the designated display region 201. The first dielectric layer 204 is formed, for example, by plasma enhanced chemical vapor deposition (PECVD) with suitable deposition parameters such that the first dielectric layer 204

covers the gate 202a and the scan line 202b inside the designated display region 201 only. Wherein, the first dielectric layer 204 has a thickness getting smaller toward the edge. The first dielectric layer is fabricated using a material such as silicon nitride (SiNx).

[Para 34] Thereafter, a channel layer is formed over the substrate 200 crossing over the gate 202a. Fig. 3A is a magnified view of section III in Fig. 2B. As shown in Fig. 3A, the first dielectric layer 204 covers the gate 202a and the scan line 202b inside the designated display region 201 and exposes the first patterned conductive layer 202 outside the designated display region 201. The channel layer 206 over the substrate 200 crosses over the gate 202a. The channel layer 206 can be a channel amorphous silicon layer. After forming the channel layer 206, an ohmic contact layer (not shown) may form over the channel layer 206 selectively. The ohmic contact layer is a n+ amorphous silicon film, for example.

[Para 35] As shown in Fig. 2C, a second patterned conductive layer 210 is formed over the substrate 200. The second patterned conductive layer 210 is formed, for example, by depositing conduct material over the substrate 200 to form a second conductive layer (not shown) and then conducting photolithographic and etching processes to pattern the second conductive layer into source/drain terminals 210a and data lines 210b. The second conductive layer is formed, for example, by sputtering a metallic material such as aluminum. Since the second patterned conductive layer 210 and the first patterned conductive layer 202 are electrically connected, possible damage due to an electrostatic discharge before forming the pixel electrode in a conventional method can be avoided.

[Para 36] To describe more fully the relative position between various films including the first patterned conductive layer 202, the first dielectric layer 204 and the second patterned conductive layer 210, refer to Figs. 3B and 3C. Fig. 3B is a simplified sectional view of Fig. 2C and Fig. 3C is a magnified view of section III' in Fig. 2C. As shown in Fig. 3B, the first patterned conductive layer 202 and the second patterned conductive layer 210 on the substrate 200 are connected through area outside the designated display

region 201. However, inside the designated display region 201, the first dielectric layer 204 isolated the two.

[Para 37] As shown in Fig. 3C, the second patterned conductive layer 210 including the source/drain terminal 210a and the data line 210b inside the designated display region 201 and the underlying first patterned conductive layer 202 including the gate 202a and the scan line 202b are separated from each other. However, the first patterned conductive layer 202 and the second patterned conductive layer are electrically connected outside the designated display region 201.

[Para 38] After forming the source/drain terminal 210a and the data line 210b, Figs. 3D and 3E show the subsequent steps for fabricating the thin film transistor array after the step in Fig. 3C.

[Para 39] As shown in Fig. 3D, a second dielectric layer 212 serving as a passivation layer is formed over the substrate 200 covering the aforementioned device. The second dielectric layer 212 has a plurality of contact openings 214 that exposes the other terminal (the drain terminal) of the source/drain terminal 210a. The second dielectric layer 212 is fabricated using a dielectric material, for example.

[Para 40] As shown in Fig. 3D, a pixel electrode 216 is formed inside the designated display region 201 filling the contact openings 214 in the second dielectric layer 212. The pixel electrode 216 is an indium-tin oxide film, for example. After the aforementioned process, an etching operation is carried out to remove the second dielectric layer 212, the second patterned conductive layer 210, the first dielectric layer 204 and the first patterned conductive layer 202 outside the designated display region 201.

[Para 41] One major characteristic of this invention is that the second patterned conductive layer and the first patterned conductive layer are electrically connected to prevent electrostatic discharge before forming the pixel electrode. Furthermore, this invention need no additional photomask step and hence able to avoid possible damage to the thin film transistor device caused by an electrostatic discharge between the electrically isolated first and second metallic layer in a conventional fabrication process.

[Para 42] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.